What is Claimed Is:

1. A network switch comprising:

a plurality of ports configured for transferring data packets;

an external memory interface configured for transferring data packets between the network switch and an external memory, the external memory interface including a scheduler for selectively assigning memory access slots of the external memory interface to ports based on respective programmable information entries.

2. The network switch according to claim 1, wherein the external memory interface includes an assignment table memory for storing the respective programmable information entries.

3. The network switch according to claim 2, wherein the programmable information entries are stored in the assignment table memory by an external controller.

~~4. The network switch according to claim 1, wherein each said programmable~~ information entry includes a port operation code, and the scheduler sets the operation of ~~the port based on the port operation code.~~

5. The network switch according to claim 4, wherein the port operation code includes one of a read bit and a write bit, the scheduler selectively assigning each of the memory access slots as are of a read slot and a write slot, based on the corresponding port operation code.

6. The network switch according to claim 1, wherein the programmable information entries include a sequence of memory access slot assignments, the scheduler assigning the memory access slots as a continuously repeating sequence based on the sequence.

7. The network switch according to claim 6, wherein one of the programmable information entries includes a wrap-around bit at an end of the sequence, the scheduler returning to a first memory access slot of the sequence upon detecting the wrap-around bit.

8. The network switch according to claim 2, wherein the assignment table memory is a RAM.

9. The network switch according to claim 2, wherein the assignment table memory is a group of registers.

10. The network switch according to claim 1, wherein a programmable information entry includes a plurality of memory access slot assignments, the scheduler selecting one of the plurality of memory access slot assignments based on one or more detected conditions.

11. A method of assigning memory access slots in a network switch to a plurality of network switch ports, each configured for transferring data packets to an external memory, the method comprising:

storing programmed memory access slot assignment information into a memory; and

selectively assigning memory access slots to the respective network switch ports based on the programmed memory access slot assignment information.

12. The method of claim 11, further comprising the steps of:

selecting a slot-to-port assignment configuration from the programmed memory access slot assignment information;

writing the selected slot-to-port assignment configuration from the memory to an assignment configuration memory within the network switch, the selectively assigning step including assigning the memory access slots to the respective network switch ports based on the selected slot-to-port assignment configuration stored in the assignment configuration memory.

~~13. The method according to claim 12, wherein the storing step comprises setting each slot-to-port assignment within the slot-to-port assign configuration to include one of a read and a write bit for indicating whether the corresponding memory access slot is one of a read and write slot.~~

14. The method according to claim 12, wherein the storing step comprises setting each slot-to-port assignment configuration as a repeating sequence of an N number of memory access slot assignments.

15. The method according to claim 12, wherein the storing step includes storing into the slot-to-port assignment configuration a wrap-around bit that returns the sequence to a first memory access slot at a start of the sequence from an "Nth" memory access slot.

16. The method of claim 11, wherein the step of selectively assigning memory access slots includes assigning memory access slots based on the programmed memory access slot assignment information having a conditional selection of port assignments.

17. A switched network system comprising:

a first memory for storing a plurality of programmable system settings;

a second memory for storing data packets;

a network switch having a plurality of ports configured for transferring data packets, the network switch including:

(1) an external memory interface configured for transferring data packets between the network switch and the second memory; and

(2) a scheduler for selectively assigning memory access slots to respective ports based on a selected one of the plurality of programmable system settings stored in the assignment table memory; and

a system controller for supplying the selected one of the plurality of system settings to the network switch.

18. The switched network system according to claim 17, wherein the external memory interface includes a slot assignment table memory.

19. The switched network system according to claim 17, wherein the programmable information includes a port operation code, and the scheduler sets the operation of the port based on the port operation code.

20. The switched network system according to claim 19, wherein the port operation code includes one of a read bit and a write bit causing the scheduler to assign memory access slots as read and write slots, respectively.

21. The switched network system according to claim 17, wherein the programmable information includes a sequence of an N number of memory access slot assignments that is continuously repeated by the scheduler in assigning memory access slots.

22. The switched network system according to claim 21, wherein the programmable information includes a wrap-around bit at an end of the sequence and the scheduler returns to a first memory access slot at a start of the sequence upon detecting the wrap-around bit.

23. The switched network system according to claim 18, wherein the assignment table memory is a RAM.

24. The switched network system according to claim 18, wherein the assignment table memory is a group of registers.

25. The switched network system according to claim 17, wherein the first memory is an EEPROM.